Process Variation Dimension Reduction Based on SVD

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ABSTRACT

We propose an algorithm based on singular value decomposition (SVD) to reduce the number of process variation variables. With few process variation variables, fault simulation and timing analysis under process variation can be performed efficiently. Our algorithm reduces the number of process variation variables while preserving the delay function with respect to process variation. Compared with the principal component analysis (PCA) method, our algorithm requires less computation time and guarantees the reduced process variation variables are independent. Experimental results on ISCAS85 circuits show that the algorithm works well.

1 INTROCUTION

In modern multi-layer VLSI circuits, the dimension of the process variation is large. For example, in a *k*-metal technology, there are *2k* variables for metal width and thickness, *k* variables for inter-layer dielectric (ILD) thickness, a gate length variable, and some other variables. With such a large number of process variation variables, timing analysis under process variation is very time consuming, and may not find the worst-case process corner [1][2].

In this paper, we propose the novel concept of variation dimension reduction. The idea is originated from the following observation. For different nets, the underlying process variation variables are the same. Therefore, the delays of the nets are correlated. We model the delay from an input pin of a cell to an input pin of a downstream cell, also known as the buffer-to-buffer delay, as a linear function of process variation variables:

$$d = d_{nominal}(1 + a_1x_1 + a_2x_2 + \ldots + a_nx_n),$$

where x_1, x_2, …, x_n are process variation variables, a_1, a_2, …, a_n are their corresponding coefficients, and $d_{nominal}$ is the nominal delay. For different nets, the coefficients are different, but the process variation variables are the same. The assumption that the delay is linear with respect to each process variation variable is supported by SPICE simulation of real circuits within reasonable ranges of the process variation [3].

There are many forms of process variation [4][5]. In this paper, we only consider systematic process variation and assume the process variation variables among different nets are fully correlated. We assume the following variation ranges: metal thickness ±20%, metal width ±10%, ILD thickness ±40%, and gate length ±10%. To obtain the delay function with respect to process variation, we first extract interconnect parasitic from the layout and compute the nominal buffer-to-buffer delay for all nets. Then for each process variation variable, we modify the layout or the technology file by varying a specified amount (for example, +10% for metal1 thickness), and perform RC extraction and delay evaluation for the modified layout. The coefficient for this process variation variable is obtained by interpolating the two delays.

Recently, the principal component analysis (PCA) method was used to reduce the dimension of process variation [7]. It was shown to be effective for analyzing analog circuits under process variation. However, the PCA method is inefficient for digital circuits, because the PCA method constructs and solves a correlation matrix of size $mn \times mn$, where n is the number of process variation variables and m is the number of nets or devices. For digital circuits, m is easily in hundreds or thousands.

In this paper, we propose a new method based on singular value decomposition (SVD) [6]. Our algorithm detects the linear dependence and reduces the number of process variation variables, while minimizing the average error of the delay. Note that although the PCA method also uses SVD, their matrix is size $mn \times mn$ while ours is size $m \times n$. To make the reduced process variables linearly/statistically independent, which is desirable for fault simulation and timing analysis, we also propose a sub-matrix SVD method.

In Section 2, the SVD method and sub-matrix SVD method for dimension reduction are given. In Section 3, we show the experimental results. It shows that if we simply pick the most important process variation variables and discard the

rest, then the average error of net delay is twice as much as the average error produced by our algorithm.

2 ALGORITHM

2.1 Singular Value Decomposition (SVD)

The SVD method is based on the following theorems [6].

Theorem 1 If A is an $m\times n$ matrix, then there exist orthogonal $m\times m$ matrix $U=[u_1,\ldots,u_m]$ and $n\times n$ matrix $V=[v_1,\ldots,v_n]$, such that $U^T\cdot A\cdot V=diag(\sigma_1,\ldots,\sigma_p)$, which is an $m\times n$ matrix, $p=\min\{m,n\}$, and $\sigma_1\geq\sigma_2\geq\ldots\geq\sigma_p\geq 0$.

The σ_i's are the singular values of A, and vectors u_i and v_i are the ith left and right singular vector, respectively. The process to find U and V is called SVD. It can be done by the Golub-Reinsch algorithm of time complexity $O(m^2n+mn^2+n^3)$ [6] (pp. 254). To compute $U(:,1:n)=[u_1,\ldots,u_n]$, which is an $m\times n$ ($m>n$) matrix, the time complexity is $O(mn^2+n^3)$ [6].

Theorem 2 Let the SVD of $m\times n$ matrix A be defined in Theorem 1. If $r<\text{rank}(A)$ and let $A^*=\sum_{i=1}^{r}\sigma_i u_i v_i^T$, then

$$\min_{rank(B)=r}\|A-B\|_2=\|A-A^*\|_2=\sigma_{r+1}.$$

In other words, A^* is the best 2-norm approximation of A among all rank r matrices.

2.2 Application to Dimension Reduction

We are given the delay of m nets represented as Ax, where A is an $m\times n$ matrix, n is the number of process variation variables, $x=[x_1,\ldots,x_n]$ is the vector of process variation variables, and x_i's are independent of each other.

From Theorem 2, $A^*=U(:,1:r)\cdot S\cdot V(:,1:r)^T$, where $S=diag(\sigma_1,\ldots,\sigma_r)$, $U(:,1:r)=[u_1,\ldots,u_r]$, and $V(:,1:r)=[v_1,\ldots,v_r]$. Therefore, $Ax\approx A^*x=U(:,1:r)\cdot S\cdot V(:,1:r)^Tx=Bz$, where $B=U(:,1:r)\cdot S$ is an $m\times r$ matrix and $z=V(:,1:r)^Tx$ is an $r\times 1$ vector. Since the dimension of B is much less than the dimension of A, we use Bz to approximate Ax.

If we just want to reduce the number of process variation variables, then Bz is the resulting delay function, and z is the vector of new process variation variables. However, we often have an additional requirement from circuit simulation that the new process variation variables $z_1,\ldots,z_r$ must be independent. For example, if $z_1=x_1-x_2+x_3$ and $z_2=x_1+x_2-x_3$, then z_1 and z_2 are not independent although the number of variables is reduced from 3 to 2.

2.3 Sub-Matrix SVD (SMSVD)

We propose a sub-matrix SVD method (SMSVD) to ensure the independence between z_i's. The basic idea is to partition columns of A into r sub-matrices, and then use SVD on each sub-matrix. The following is the algorithm:

1) Partition A into sub-matrices $A_1, A_2, \ldots, A_r$, where $A=[A_1, A_2,\ldots, A_r]$. A_i is an $m\times q_i$ matrix, $i=1,\ldots, r$.
2) For $i=1,\ldots, r$, compute the approximation matrix A_i^* of A_i through SVD in which the approximation rank is 1. Define SVD of A_i as $U_i^T\cdot A_i\cdot V_i=diag(\sigma_{i1},\ldots,\sigma_{ip})$, then $A_i^*=U_i(:,1)\cdot\sigma_{i1}\cdot V_i(:,1)^T$ and $\|A_i-A_i^*\|_2=\sigma_{i2}$.
3) Construct $B=[U_1(:,1)\sigma_{11}, U_2(:,1)\sigma_{21}, \ldots, U_r(:,1)\sigma_{r1}]$,
$$z=Cx=\begin{bmatrix}z_1\\z_2\\\vdots\\z_r\end{bmatrix}=\begin{bmatrix}V_1(:,1)^T & 0 & \ldots & 0\\0 & V_2(:,1)^T & \ldots & 0\\\vdots & \vdots & \ddots & \vdots\\0 & 0 & \ldots & V_r(:,1)^T\end{bmatrix}\begin{bmatrix}\boldsymbol{x_1}\\\boldsymbol{x_2}\\\vdots\\\boldsymbol{x_r}\end{bmatrix},$$
where B is an $m\times r$ matrix, C is an $r\times n$ matrix, $\boldsymbol{x_i}$ is a $q_i\times 1$ vector, $i=1,\ldots,r$, and $B\cdot C=[A_1^*, A_2^*, \ldots, A_r^*]$.

It is easy to see that z_i's are independent since x_j's are independent for $j=1,\ldots,n$, and $\boldsymbol{x_i}$'s are independent for $i=1,\ldots,r$.

The error of approximating Ax by Bz can be evaluated through $\|A-B\cdot C\|_2$. We can prove the following upper bound on the error.

Theorem 3 Given net delay matrix Ax, we can use SMSVD to compute B, C and z such that

$$\|A-B\cdot C\|_2\leq\sqrt{r}\max_i\sigma_{i2},$$

and z_i's are independent. The time complexity is

$$O(r\cdot(m\cdot\max_i(q_i)^2+\max_i(q_i)^3)).$$

Proof After SMSVD, we have $A_i^*=U_i(:,1)\cdot\sigma_{i1}\cdot V_i(:,1)^T=U_i\cdot diag(\sigma_{i1},0,\ldots,0)\cdot V_i^T$, where U_i is an orthogonal $m\times m$ matrix, V_i is an orthogonal $q_i\times q_i$ matrix and $diag(\sigma_{i1},0,\ldots,0)$ is an $m\times q_i$ diagonal matrix, $i=1,\ldots,r$. Thus,

$B\cdot C=[A_1^*, A_2^*,\ldots, A_r^*]$

$=[U_1\cdot diag(\sigma_{11},0,\ldots,0)\cdot V_1^T,\ldots,U_r\cdot diag(\sigma_{r1},0,\ldots,0)\cdot V_r^T]$,

and $A-B\cdot C$

$=[U_1\cdot diag(0,\sigma_{12},\ldots,\sigma_{1p})\cdot V_1^T,\ldots,U_r\cdot diag(0,\sigma_{r2},\ldots,\sigma_{rp})\cdot V_r^T]$.

Let

$$D=\begin{bmatrix} diag(0,\sigma_{12},\ldots,\sigma_{1p}) & 0 & \ldots & 0 \\ 0 & diag(0,\sigma_{22},\ldots,\sigma_{2p}) & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & diag(0,\sigma_{r2},\ldots,\sigma_{rp}) \end{bmatrix},$$

then $A-B\cdot C=[U_1,\ldots,U_r]\cdot D\cdot\begin{bmatrix} V_1^T & 0 & \ldots & 0 \\ 0 & V_2^T & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & V_r^T \end{bmatrix}$. The 2-norm of matrix $\begin{bmatrix} V_1^T & 0 & \ldots & 0 \\ 0 & V_2^T & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & V_r^T \end{bmatrix}$ is 1, and 2-norm of matrix D is $\max_i \sigma_{i2}$. Furthermore, $[U_1,\ldots,U_r]=$

$$U_1\cdot\underbrace{[I_m,\ldots,I_m]}_{r}\cdot\begin{bmatrix} I_m & 0 & \ldots & 0 \\ 0 & U_1^TU_2 & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & U_1^TU_r \end{bmatrix},$$ where I_m is an $m\times m$ identity matrix, U_1 and $\begin{bmatrix} I_m & 0 & \ldots & 0 \\ 0 & U_1^TU_2 & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & U_1^TU_r \end{bmatrix}$ are orthogonal matrices. Since the 2-norm of $\underbrace{[I_m,\ldots,I_m]}_{r}$ is $\sqrt{r}$, and 2-norm of an orthogonal matrix is 1, then the 2-norm of $[U_1,\ldots,U_r]$ is $\sqrt{r}$.

Therefore, $\|A-B\cdot C\|_2 \le \sqrt{r}\max_i \sigma_{i2}$.

The time complexity is given by [6]. ♦

A good partition method that minimizes the value of $\max_i \sigma_{i2}$ can reduce the error of SMSVD. We will give a partition scheme and prove an upper bound for $\max_i \sigma_{i2}$.

Theorem 4 Let $a_1,\ldots,a_n$ be singular values of each column of matrix A and assume without loss of generality $a_1\ge a_2\ge\ldots\ge a_n$. There exists a partition such that

$$\max_i \sigma_{i2} \le ((a_r^2+a_{r+1}^2+\ldots+a_n^2)/2)^{1/2},$$

where r is the reduced dimension.

Proof Assume the singular values of any $l\times k$ matrix M are $\sigma_1,\ldots,\sigma_k$, where $\sigma_1\ge\ldots\ge\sigma_k\ge 0$, the singular value of column i of matrix M is b_i, $i=1,\ldots,k$. Then it is well known that $b_1^2+b_2^2+\ldots+b_k^2=\sigma_1^2+\sigma_2^2+\ldots+\sigma_k^2\ge 2\sigma_2^2$. Thus,

$$\sigma_2\le((b_1^2+b_2^2+\ldots+b_k^2)/2)^{1/2}.$$

To reduce the dimension of A to r, let A_i contain a single column whose singular value is a_i for $i=1,\ldots,r-1$, and A_r contain all the other columns. Then

$$\max\{0,\ldots,0,\sigma_{r2}\}=\sigma_{r2}\le((a_r^2+a_{r+1}^2+\ldots+a_n^2)/2)^{1/2}.\ \blacklozenge$$

The above proof also implies that to further reduce the error of SMSVD, we need to find a column combination that minimizes $\max_i(a_{i1}^2+a_{i2}^2+\ldots+a_{ik}^2)$. This problem is NP-complete for $r=2$ and strongly NP-complete for $r\ge 3$ [8]. We use the following heuristic:

- Compute the singular value for each column of A.
- Select r columns A_1, A_2, …, A_r that contains the r maximum singular values. Put A_1, A_2, …, A_r into r different groups and delete these columns from A.
- Repeat the above process until A is empty.

3 EXPERIMENTAL RESULTS

We first performed physical layout for ISCAS85 circuits using TSMC 0.25um 5 metal technology. After the preliminary processing, we have 12 process variation variables. Gate length is not included in this experiment since for 0.25um technology, gate length variation dominates all other process variation. Commercial parasitic extraction tools are used to extract parasitic and to compute all buffer-to-buffer net delays in each circuit (only for rising input). The delays of the nets are represented as linear functions of process variation variables.

Using the SMSVD algorithm, we reduce the number of process variation variables from 12 to 3. The 3 new variables are independent of each other. To demonstrate the efficiency of SMSVD, we compare the errors of the delays with the method MAX3, which selects three process variation variables that have the greatest impact on the delays. (In this experiment, the three process variation variables are ILD1, medal2 thickness and medal2 width.) Table 1 compares the error of delay for all nets in the ISCAS85 circuits. The process variation ranges are ±10%. The approximation error is defined as follows. For each net, let the accurate delay function be

$$d=d_{nominal}(1+a_1x_1+a_2x_2+\ldots+a_nx_n).$$

Let the delay of our SMSVD approximation be $d_1=d_{nominal}(1+b_1z_1+b_2z_2+b_3z_3)$. Then the error of SMSVD for the net is $(d-d_1)/d$. Similarly, let the delay of MAX3 be $d_2=d_{nominal}(1+a_1x_1+a_2x_2+a_3x_3)$. Then the error of MAX3 for the net is $(d-d_2)/d$. For each circuit, the CPU time for SMSVD algorithm is 0.1sec to 0.7sec. From the table, we can see that SMSVD reduces the range, mean and standard deviation of relative errors of net delays.

Table 1 Approximation error for ISCAS85 Circuits

Circuit (# of nets)	SMSVD			MAX3		
	Range	Mean	Std Dev	Range	Mean	Std Dev
C432 (335)	−2.9% +1.9%	0.15%	0.28%	−3.4% +3.1%	0.30%	0.52%
C499 (852)	−3.9% +6.0%	0.28%	0.55%	−9.6% +3.1%	0.45%	0.81%
C880 (699)	−9.4% +8.1%	0.26%	0.69%	−12% +6.3%	0.51%	0.90%
C1355 (1074)	−6.9% +6.4%	0.31%	0.74%	−9.6% +5.0%	0.52%	0.94%
C1908 (822)	−3.0% +6.0%	0.20%	0.42%	−4.0% +4.4%	0.42%	0.51%
C2670 (1478)	−5.1% +2.7%	0.18%	0.41%	−13% +3.2%	0.48%	0.82%
C3540 (2044)	−4.0% +5.1%	0.19%	0.39%	−13% +6.3%	0.50%	0.73%
C5315 (3218)	−5.0% +5.0%	0.19%	0.38%	−13% +4.4%	0.50%	0.71%
C6288 (4630)	−6.8% +5.3%	0.18%	0.38%	−9.6% +6.8%	0.41%	0.46%
C7552 (3709)	−5.5% +6.9%	0.39%	0.85%	−6.7% +7.7%	0.63%	0.90%

4 CONCLUSIONS

An algorithm to reduce the dimension of process variation is presented and the error bound is proved. The experiment shows the algorithm successfully reduces the number of process variation variables while preserving the independence among new process variation variables and the range of the delay function. The new method is applied on ISCAS85 circuits and show good performance in both range and accuracy.

The main advantage of our method over the PCA method is that the PCA method performs SVD for the correlation matrix of size $mn \times mn$, while our algorithm performs SVD for the delay matrix of size $m \times n$.

Acknowledgement

This research is supported in part by SRC grant 2000-TJ-844, NSF grants CCR-0098329, CCR-0113668, EIA-0223785, ATP grant 000512-0266-2001, and a fellowship from Applied Materials.

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